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EIC Detector R&D Progress Report

Project ID: eRD25
Project Name: Silicon Tracking and Vertexing Consortium
Period Reported: August 2020 to March 2021
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Abstract

The eRD25 proposal builds upon the prior work of eRD16 and eRD18, and benefits from a collaboration with CERN to develop a sensor for a future upgrade of the inner tracking system of the ALICE experiment. The possibility of higher granularity and lower power consumption offer considerable advantages for an EIC tracking detector in terms of both improved momentum resolution and vertex reconstruction resolution. The performance of the inner tracking system will have a direct impact on several key observables at the EIC, which will be constrained by the performance of the inner tracker. These include the precision measurement of the scattered electron in DIS, the reconstruction of heavy-flavour decays and the measurement of the charged constituents of jets. This proposal presents a design path to an EIC silicon tracking detector starting with the development of the sensor itself.

1. Project aim and motivation

Before presenting a report on the work completed so far in FY21 and plans for the remainder of this funding period and beyond, we would like to briefly summarise aim and motivation of the project.

eRD25 aims to prepare the ground for the development of a well-integrated and large-acceptance EIC Silicon Vertex and Tracking (SVT) detector concept, based on Monolithic Active Pixel Sensors (MAPS) in a commercial 65 nm CMOS imaging process. The sensor technology choice is driven by both the required physics performance and the development opportunity exploiting synergies with the ALICE ITS3 project.

Our extensive set of simulations have demonstrated that vertexing and tracking requirements at the EIC will not be met unless an aggressive detector concept is developed based on the high granularity (10 μm pixel pitch) and extremely low material budget (0.05% X_0 per layer) targeted by the ITS3 project with a new generation MAPS sensor at the 65 nm node.

The compatible technological solutions and timescales of the ITS3 and EIC projects allow the EIC to leverage on a large collaborative effort at CERN to significantly reduce time, effort, risk and cost associated to the development of the EIC SVT sensor and detector infrastructure, while giving access to an advanced CMOS technology with improved performance, crucial to deliver the EIC science programme, and guaranteed process availability on the EIC project timescale.

Our baseline SVT design is thus an ITS3-derived detector concept. In the vertex layers, we foresee the use of the wafer-scale ITS3 sensor and of the ITS3 detector concept for ultra-low mass (i.e., low power, wafer-scale, thin sensors bent around the beam pipe). For the tracking layers and disks, an ITS3-derived sensor will be developed to optimize sensor size versus yield to cover larger areas, together with dedicated engineering solutions for design of low mass staves and disks.

Work in collaboration with ITS3 has already started and the current status of the project is presented in the remainder of the report.

2. Past

2.1 What was planned for this period?

As stated in our July 2020 proposal, the aims of the eRD25 consortium for FY21 are

- Joining the emerging ALICE ITS3 R&D program on 65 nm technology to gain the required expertise to design a (ITS3-derived) MAPS sensor for the EIC;
- Developing and investigating the performance of well-integrated and large-acceptance tracking concepts with barrel layers and forward/backward disks;
- Identifying areas requiring targeted services R&D;
- Growing eRD25 into an EIC Silicon Consortium (EICSC) to address all aspects of the development of an ITS3-derived EIC SVT detector.

2.2 What was achieved?

During the reported period work has progressed as planned on all proposed activities as described in the following sections.

2.2.1 Sensor development

During the reported period we have actively engaged with design activities being undertaken by the ITS3 Work Package 2 (WP2) on sensor design in the TowerJazz 65 nm CMOS imaging process (ISC). The first ITS3-WP2 activity was to submit an MLR (Multi-Layer Reticle – a process in which multiple layers are fabricated on the same

mask, trading silicon area for reduced cost) for fabrication. This submission is referred to as MLR1 and it targeted structures for technology exploration, to assess the performance of this new technology process for MAPS design, and prototype IP blocks that would be required by a future sensor.

The MLR1 comprises transistor test structures, analogue and digital pixel test structures, rolling shutter matrices, charge-sensitive amplifier prototypes, bandgap circuits, temperature sensor, LVDS receiver and CML transmitter, ring oscillators. These were provided by a large number of groups (CERN, IPHC, CPPM, NIKHEF, DESY, RAL, Yonsei). The RAL contribution to MLR1 is the LVDS receiver and CML line driver for use in the digital output stage of the final sensor. The MLR1 was submitted to the foundry on December 1st and is expected back in late Q2 2021. Testing can then begin, and preparations for this are already underway (see 3.1.1). A snapshot of the layout of MLR1 is shown in Figure 1.

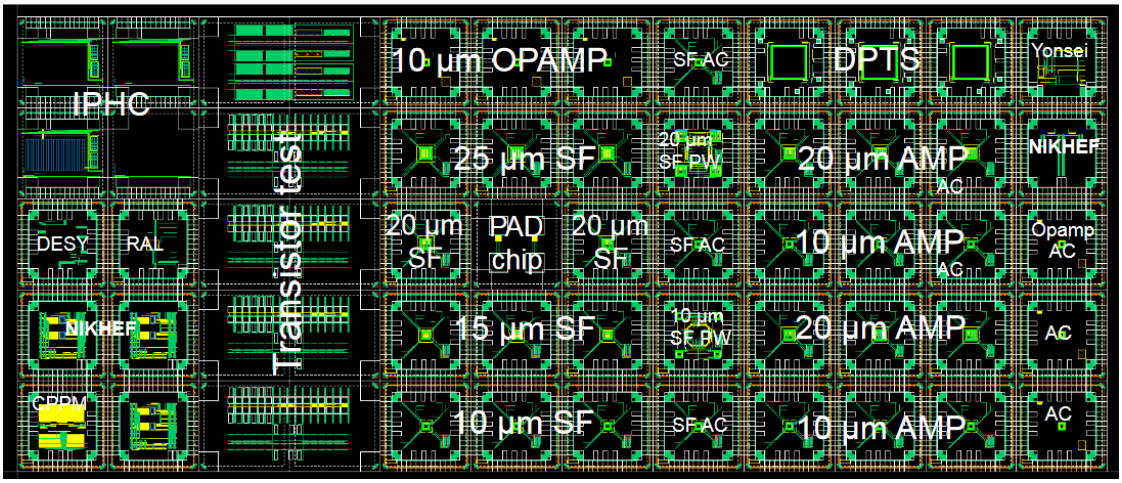

Figure 1: MLR1 layout.

The advantages of pursuing this collaborative effort are strongly illustrated by the completion of MLR1. We were able to complete and submit a chip containing many more blocks than we could have produced working alone, on a relatively short time scale. Similarly, access to such an advanced technology is only possible thanks to this collaboration.

2.2.2 Services

Following on from estimation and parameterisation of the service loads for the proposed detector concept prepared in the context of the EIC Yellow Report (YR) and presented in July 2020 [1, 2], work during the reported period concentrated on the largest mass in the services, that is, by far, the power supply and return cabling. Reducing this can be addressed in multiple ways. The most obvious avenue to explore is reducing the power required by the sensors and this is being addressed with the choice of a sensor in 65 nm technology, as this process offers significant improvements in power consumption with respect to older technology generations. An EIC sensor based on the ITS3 type development is expected to reduce the power needed by half with respect to the ALPIDE, to a dissipation of 20 mW/cm^2.

As the voltage supplied to the sensors is also reduced from 1.8V to 1.2V, to maintain the cable voltage drops to manageable levels, a significant fraction of the conductor is still required. It is possible to reduce the radiation length of the power cabling by

moving to copper clad aluminium conductors. This can help significantly since the X_0 of aluminium is approximately a factor of six lower than the X_0 of copper. Using aluminium conductors unfortunately comes at a cost in space required by the services since the conductivity of aluminium is about 65% that of copper. The impact of choosing aluminium conductors has been estimated in the parametrisation presented earlier.

Another option would be to significantly reduce the number of required conductors to power the detector. This could be addressed by either serial powering of detector staves, or the integration of radiation tolerant DC-DC converters at the stave ends. We have completed an initial exploration of the reductions in service loads that could be seen from these powering options and the results are very promising. The scenarios investigated focused on the use of the FEASTMP radiation and magnetic field tolerant DC-DC converters available from CERN and the longer-term development of a serial powering scheme using the on-chip Shunt-LDO regulator developed for deployment at the HL-LHC. Several different architectures were evaluated in both cases and the results presented as the fractional reduction in mass that could be expected as compared to a LDO regulated power scheme as is used in the ALICE ITS2. For reasonable architectures using these scenarios, the in-detector cabling mass could be reduced by up to 60% and 90% inside and outside the active detector volume based on architectures using DC-DC converters or serial powering schemes. The complete study can be found at [3,4].

2.2.3 Physics simulations

Extensive GEANT-based simulations have been pursued by H. Wennlöf in Birmingham and by R. Cruz-Torres in Berkeley to quantify the tracking and vertexing performance of hybrid-silicon and all-silicon charged-particle detector. These simulations are at the basis of the two baseline tracking concepts presented in the YR. In addition to single-track momentum resolutions and displacements, studies were performed, for example, of the track angular resolutions at the interface of the tracker(s) to the particle-identification systems as well as of several physics processes. We briefly present the two baseline concepts and then highlight a few examples.

The two YR tracking concepts shown in Figure 2 below have been tested against the combined physics requirements on pointing resolution, momentum resolution, and other quantities from the YR Physics Working groups. Both concepts feature a pixel pitch of 10 μm and our material budget estimates. Our simulation results show that the requirements on pointing resolution can be met in all regions with the proposed layouts and the ITS3-like technology despite the challenges imposed by the diameter of the EIC beampipe. The relative momentum resolution presents challenges in particular in the regions of high (absolute) η within the space available for the innermost tracking system with the currently envisioned solenoidal magnetic field configurations aligned with the electron beam, in particular for a 1.5 T (maximum) magnetic field strength and despite the 10 μm pixel pitch of our low-mass concepts.

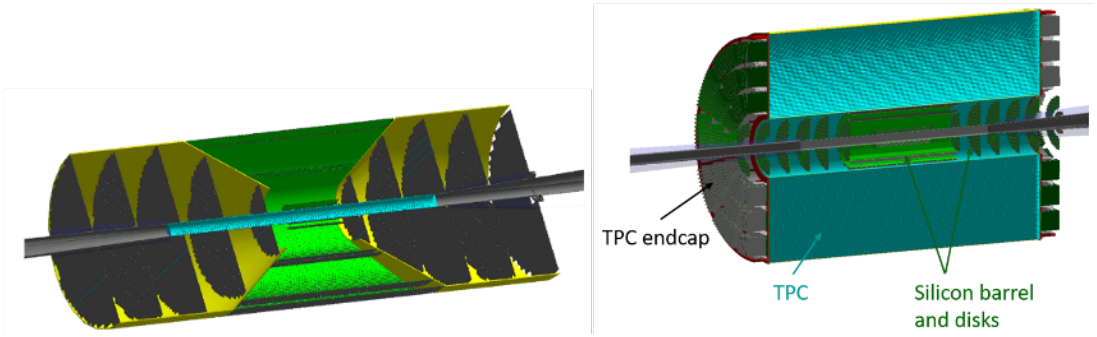

Figure 2: EIC Yellow Report EIC SVT baseline concepts. Left: all-silicon. Right: hybrid-silicon. Both concepts span -1.2 < z < 1.2 m along the beamline. The all-silicon concept has an outer radius of approximately 0.4 m, whereas the hybrid-silicon concept has a larger radius of approximately 0.9 m.

Studies have been made by H. Wennlöf using D mesons produced in ep collisions generated in Pythia 8, at the collision energies suggested by the YR Physics Working Group, to investigate the open charm event reconstruction capabilities of different tracker designs in a GEANT4 simulation. The D^0, D^+, and D^{*+} invariant masses were reconstructed through their decays to pions and kaons, and the mass peak resolution and signal over background ratio of the peaks were extracted through fits. This was done for four different tracker designs: the silicon plus TPC (hybrid) YR baseline, and three all-silicon designs with different outer radii based on previous EICRoot simulations summarised in [5]. Figure 3 shows the resulting mass peak width for D^0 mesons for four different electron-proton energy combinations. Filled lines represent a 1.5 T solenoidal field, and dashed lines represent a 3.0 T solenoidal field. From this, it can be seen that a 3 T magnetic field improves the mass resolution for all the tested energies and concepts. It can also be seen that the hybrid baseline outperforms the tested all-silicon concepts when using this metric. As the pions and kaons from the studied D^0 decays have low transverse momentum (< 3 GeV/c), this agrees with previous results where hybrid concepts have been shown to have better momentum resolution than all-silicon concepts at transverse momenta below ~5 GeV/c [5]. There is little performance difference between the tested all-silicon layouts (note that these are different layouts with respect to the YR baseline all-silicon concept that is discussed below). Details of this study, and further studies including other D mesons, are being prepared for publication in Wennlöf's PhD thesis.

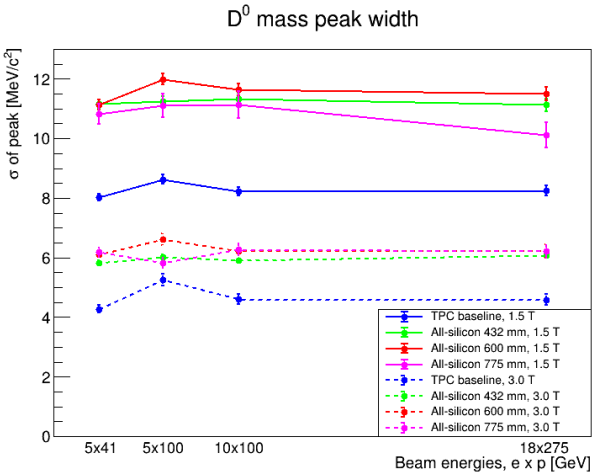

Figure 3: Fitted Gaussian sigma of the reconstructed D^0 invariant mass peak, for different tracker designs and magnetic fields at four different ep collision energies.

A separate set of GEANT-based studies were pursued by M. Kelsey of resolutions in topological reconstructions and to develop metrics for fast simulations that are at the basis of many of the physics studies in the YR. Prior to these studies, EIC physics assessment of e.g., the heavy-flavor structure functions, had not considered realistic topological efficiencies differentiated by e.g., the number of tracks in the collision. Figure 4 shows the correspondence that was achieved between the GEANT-based and fast simulations for topological variables in the reconstruction of D^0 mesons in simulated 18 GeV electron collisions on 275 GeV protons using the Pythia-8 event generator with an event-level cut on the deep-inelastic scattering scale $Q^2 > 1$ GeV^2 for a default configuration of the all-silicon tracker concept. The agreement between GEANT-based and full simulations is good. It leads to topological efficiencies that increase with increasing transverse momentum and are nearly uniform within the considered pseudorapidity range. This presents an important advance in the fidelity of fast simulations to project physics capability, including studies of the charmed structure function F_2, the polarization of gluons in the nucleon, and transverse momentum-dependent distributions [6].

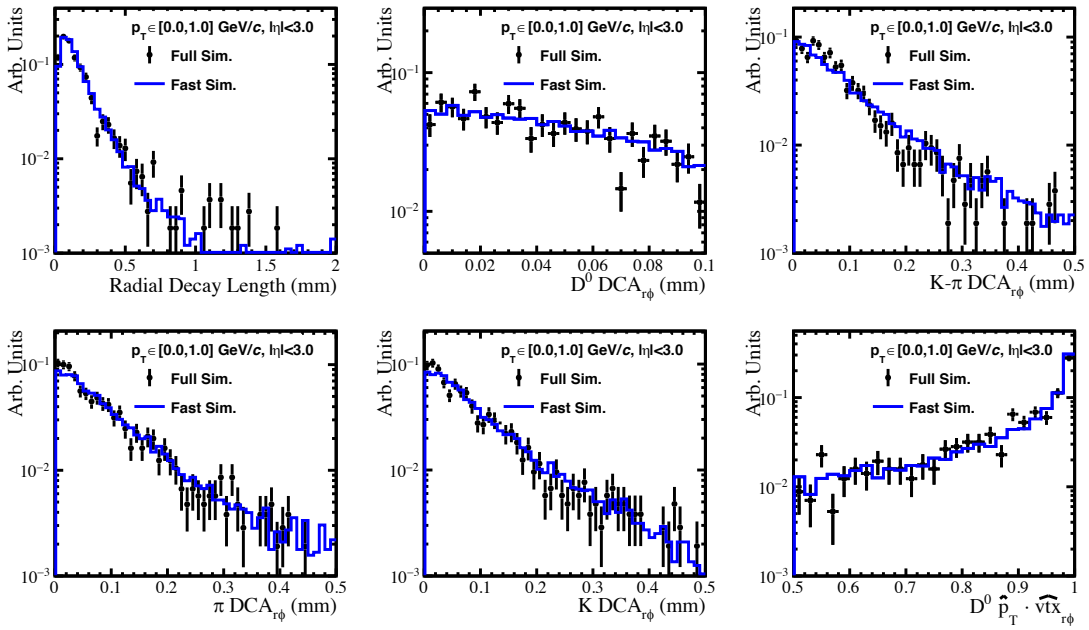

Figure 4: Comparison of reconstructed D^0 topological variables from GEANT-based simulations of an all-silicon tracking concept (points) and from fast simulation (histograms). The distributions are normalized to have unit area.

2.2.4 EIC Silicon Consortium

Activities towards the formation of the EIC Silicon Consortium have continued where the first step was to submit an Expression of Interest to the call organised by the EIC Users Group [7]. This has been signed by LBNL, University of Birmingham and Rutherford Appleton Laboratory on behalf of UK institutions, BNL Instrumentation Division, CCNU (Wuhan), JLab, ORNL, Institute of Modern Physics (IMP, China). By now groups from Italy and France have expressed interest in joining. Many of the members of the EICSC have extensive experience in the specific areas needed and were instrumental in the development of similar MAPS based tracking detectors for STAR and ALICE.

As the requirements for vertex and tracking at the EIC and our proposed ITS3-derived EIC SVT concepts have matured driven by the completion of the YR, the full scope of the required set of R&D tasks and their associated timeline to realise the SVT is now well defined. We are thus starting a set of regular meetings and are proceeding to develop task lists and work packages (WP) that will carry out this effort.

In parallel, we have continued our engagement with the ITS3 project to prepare the path for more EICSC groups to join the relevant work packages. LBNL, BNL and Brunel University have requested access to technology Non-Disclosure Agreement (NDA) and Process Design Kit (PDK) to start work towards the MLR2 and we started participation in the ITS Work Package 3 meetings that are concerned with sensor testing. We expect to join more ITS3 work packages on sensor thinning, bending and interconnection, and mechanics and cooling as our WP structure is defined and tasks assigned.

2.3 What was not achieved, why not, and what will be done to correct this?

At this stage the project is on track to deliver the proposed FY21 programme of work.

2.4 How did the COVID-19 pandemic and related closing of labs and facilities affect progress of your project?

The work planned for this period was not affected by the closing of labs as it did not have a component that required access to lab facilities for use of equipment.

2.5 How much of your FY21 funding could not be spent due to pandemic related closing of facilities?

Not applicable, see 2.4. Note however that FY21 funding is allocated for MLR1 testing and MLR2 design and submission so it will be spent later in the year. The MLR1 design and submission have been paid with repurposed eRD18 funding.

2.6 Do you have running costs that are needed even if R&D efforts have paused?

Not applicable.

3. Future

3.1 Planned activities to complete FY21 proposed programme of work

3.1.1 Sensor development

For the development of the sensor, two tasks are now foreseen. The first is the testing of the chips resulting from the MLR1 submission. Testing is organised by the ITS-WP3 and will involve functional testing of the IP blocks and performance testing of the pixel structures. RAL will undertake testing of the LVDS-CML block they designed, where irradiation facilities at Birmingham and LBNL will be used for TID and SEE studies. Birmingham and LBNL are already engaging in the ITS3-WP3 discussions and following plans to be involved in the testing of more structures, in particular pixel test structures, where again we offered our facilities for irradiations studies. We also expect to purchase readout systems developed by the ITS3-WP3 to carry out characterisation in our laboratories.

In parallel with this, work on MLR2 is starting and will be largely completed in the remainder of this funding period. Since stitching (building chips larger than a single CMOS reticle) is critical to the ITS3 project, it is planned that the next submission, MLR2, will include a stitched sensor. Planning for this is at an early stage and the architecture is still being discussed, and involvement of each group. As the only current member of the consortium with stitching experience, RAL are currently providing guidance on this element.

3.1.2 Services

We intend to continue our investigations of the powering system options, refine the estimates of the mass required and begin prototyping some of the more promising architectures to measure the operational characteristics as relate to the noise and other properties that influence the operation of the sensors. This work should proceed apace with the sensor development. In addition, as the expected power dissipation of the 65nm sensors will be significantly less (~50%) than what is seen in the current ALPIDE generation of sensors, we hope to investigate lower mass cooling schemes.

3.1.3 Physics simulations

We intend to continue our simulation efforts in the context(s) of the imminent formation of detector collaborations and the corresponding specific detector designs now that the YR efforts have been completed. eRD25 believes that the MAPS-based concepts under its consideration have broad applicability in general purpose detector concepts for the

EIC and is thus largely agnostic to one interaction region or another, or specific proto-collaborations. Integration into the overall detector concepts, including services and supports, will thus require attention as potentially will asymmetric barrel and disk layouts if the nominal interaction point will be displaced from the origin at one or more of the interaction regions.

3.1.4 EICSC

In the next few months, we aim to fully transition eRD25 into the EICSC to start work on all aspects of the proposed EIC SVT design, fully engage with the ITS3 project and in view of the new funding scheme for EIC detector R&D and of the upcoming call for detector proposals.

One of the most urgent activities of the EICSC in the next few months will be to discuss involvement in the MLR2. This will need to be planned to give us as much insight as possible in the stitched sensor design that will be the base for further sensor development. As we will need to fork-off the ITS3 sensor development for the EIC tracking layers and disks, the common submissions will need to build a base of expertise to allow us further independent development in the future.

The other main activity of the EICSC will be engagement with the upcoming call for the detector proposals. Here it should be stated clearly that we currently do not foresee the EICSC to become part of a specific detector collaboration. We plan to keep it open to institutes from different emerging collaborations interested to work on the proposed sensor solution for their specific EIC detector implementation. This will maximise the successful delivery of the technology with the lowest cost to the project.

3.2 Plans beyond the next funding cycle

See summary document.

3.3 What are critical issues?

The critical issue for this development is availability of adequate funding on the required timescale for the development of the sensor and all other aspects of detector R&D. The ITS3 project is moving forward on a more aggressive schedule than originally planned and EIC SC groups need to join now. Whilst some EICSC institutes are involved in ITS3, this is not the case for all.

It is also worth mentioning that the funds we obtained for FY21 are below the minimum funding scenario request we presented, limiting significantly our involvement and gain of expertise in the 65 nm technology and its development for EIC application. Thus far we have been able to mitigate this with carry-over of remaining eRD16 and eRD18 funds. Overall, the project also relies heavily on resources, mostly person power, provided in-kind by Birmingham, LBNL and RAL. This will not be an adequate scale of funding to sustain future sensor design and detector development activities.

4. Additional information

No additional information.

5. Personnel

Lawrence Berkeley National Laboratory

The dominant part of the simulation efforts during this reporting period were carried out part-time by postdoctoral researchers R. Cruz-Torres and M. Kelsey. No eRD25 (or

eRD16) funds were used. Most simulations were performed within the Fun4All framework. Cruz-Torres and Kelsey were stationed at LBNL for most of the reporting period and were supervised by B.V. Jacak and X. Dong, respectively. The sensor, powering, and services efforts during this reporting period were carried out part-time by A. Collu and L. Greiner.

University of Birmingham
Dr. L. Gonella spends approximately a fraction of 0.2 FTE on the project at no cost. Prof. P. Jones and Prof. P. Newman spend approximately a fraction of 0.1 FTE on the project at no cost. They supervise two PhD students, H. Wennlöf and S. Maple, who work full time on the project, fully funded by the School of Physics and Astronomy of the University of Birmingham. Prof. P. Allport has an advisory role and participates in our regular project meetings to monitor progress.

RAL CMOS Sensor Design group
I. Sedgwick (or other chip designer) works on the project according to the awarded funding. N. Guerrini has an advisory role and participates in our regular project meetings to monitor progress.

6. External funding

Lawrence Berkeley National Laboratory
Several LBNL staff members and colleagues from other University of California (UC) campuses are part of a successful pilot project as the outcome from our response to a 2019 UC Multi-campus Research Funding Opportunity (MRPI). Although the work reported here was not funded directly through this UC proposal and Laboratory staff cannot be supported through this opportunity, closely related work has been performed in the context of the YR with MRPI funds. Our follow-on 2021 MRPI proposal was recently awarded. Even though no work reported here was funded by this MRPI proposal, we anticipate productive synergies going forward.

B.V. Jacak was named a 2019 Distinguished Scientist Fellow by the U.S. Department of Energy. This award has made it possible to attract postdoctoral researcher R. Cruz-Torres, who has performed a number of simulations contained in this work. This award has funded also undergraduate students who have performed closely related simulations.

As reported previously, A. Collu and several other LBNL staff members submitted a FY21 LDRD proposal aiming to pursue and address several key issues related to the development, interconnection and powering of larger than reticle size and up to wafer-scale sensors in the TowerJazz 65nm CMOS process for EIC purposes. This proposal was not successful.

University of Birmingham
The University of Birmingham provides funds to support two 3.5-year Ph.D. studentship was taken up by H. Wennlöf and S. Maple in September 2017 and September 2020 respectively.

In addition, our bid to support some of the R&D elements of this proposal through EU Horizon 2020 has been successful. This formed part of the NextDIS work package

included in the STRONG-2020 proposal. The proposal has been awarded €62.5k to support the submission of an EIC MAPS sensor prototype.

A UK EIC-project, proposed by us, has been invited to participate as a Preliminary Activity to the UKRI Infrastructure Fund. The proposal, submitted by a collaboration of UK institutes from nuclear and particle physics (PI: P. Jones, Birmingham, and D. Sokhan, Glasgow), is structured around detector R&D for vertex and tracking, polarimetry, and far-forward detectors. Funding has been requested for three years, starting in 2021-22. The Universities of Birmingham and Liverpool, and STFC Daresbury, RAL PPD and RAL CMOS Sensor Design group have requested approximately £2.7M to develop an R&D programme to design an EIC-specific MAPS sensor in 65 nm technology, readout systems, cooling and mechanical design. Response and confirmation of allocated funding are still awaited.

7. Publications

8. References

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3. A. Collu, Silicon vertex detector power distribution, https://indico.jlab.org/event/400/contributions/6544/, EIC SVT workshop, September 2020
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